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10/655,892	09/04/2003	Joseph Weiyeh Ku	200309451-1	1906

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EXAMINER	
STEVENSON, ANDRE C	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/655,892	KU, JOSEPH WEIYEH	
	Examiner	Art Unit	
	Andre' C. Stevenson	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6-26 and 28* is/are rejected.

7)☒ Claim(s) *2,5,27,29 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims #1 and 11 are rejected under 35 U.S.C. 102(b) as being unpatentable by Soh et al. (U.S. Pat. No.6,060,895 , Patented 05/09/00, Filed 04/20/98).

Soh teaches, in a similar method for a wafer level dielectric test structures, in figures #1 through 6 and corresponding test, with respect to **claim #1 and 11**, a method of preparing an integrated circuit (1C) **(column 6, lines 27-48)** for thermal testing **(test structure, item #30)**, a method comprising: designing a layout of the IC to include a temperature generation device **(figure #3 & 4, items #30 & 40)** to be positioned within the IC, wherein the temperature generation device **(item #11)** functions for a primary purpose of affecting a temperature at the IC and constructing the IC with the temperature generation device positioned within the IC **(fig. 2, 2a and 5; column 3, lines 63-67; column 4, lines 1-11 and line 33-44; column 5, lines 57-67; column 6, lines 1-12),** for the purpose of sensing the temperature at the IC **(column 2, lines 60-67; column 3, lines 1-5; column 4, lines 45-65).**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Soh et al. (U.S. Pat. No.6,060,895 , Patented 05/09/00, Filed 04/20/98), and in view of Mok et al. (U.S. Pat. No.6,791,171 , Patented 09/14/04, Filed 06/28/02).

Soh substantially shows the claimed invention, as stated in the text and drawings listed above.

Soh fails to show, with respect to **claim #8**, a method further comprising the step of locating the IC within an IC wafer. Soh also fails to show, with respect to **claim #9**, a method, further comprising the step of separating the IC from an IC wafer, creating an independent IC device. Finally, Soh fails to show, with respect to **claim #10**, a method further comprising the step of positioning the IC on a circuit board that is populated with peripheral devices, which would be present during actual operation of the IC.

Mok teaches, in a similar method for testing ad packaging integrated circuits, in figures 1-79 and corresponding text, in a method for preparing integrated circuit for thermal testing, ***pertaining to claim #8***, a method further comprising the step of locating the IC within an IC wafer **(fig. #18; column 21, lines 16-24)**. ***Pertaining to claim #9,*** Mok teaches, a method, further comprising the step of separating the IC from an IC wafer, creating an independent IC device **(column 21, lines 34-39)**. ***Pertaining to claim #10,*** Mok teaches, a method further

comprising the step of positioning the IC on a circuit board **(column 21, lines 9-15)** that is populated with peripheral devices, which would be present during actual operation of the IC **(column 22, lines 54-67).**

It would have been obvious to one having ordinary skill in the art at the time the invention was made, with respect to **claim #8**, to include a method further comprising the step of locating the IC within an IC wafer, into the method of Soh, as taught by Mok, with the motivation, as stated by Mok (column #22, lines #13 through 18), to allow the test and burn of integrated circuit dice (items #44 & 100) after packaging and singulation (Item #122), making it possible to detect assembly, saw and handling caused defects, while keeping the die in position for precision handling with massive parallelism.

It would have been obvious to one having ordinary skill in the art at the time the invention was made, with respect to **claim #9**, to include, a method, further comprising the step of separating the IC from an IC wafer, creating an independent IC device, into the method of Soh, as taught by Mok, with the motivation, as stated by Mok (column #22, lines #13 through 18), to allow the test and burn of integrated circuit dice (items #44 & 100) after packaging and singulation (Item #122), making it possible to detect assembly, saw and handling caused defects, while keeping the die in position for precision handling with massive parallelism.

It would have been obvious to one having ordinary skill in the art at the time the invention was made, with respect to **claim #10**, to include a method further comprising the step of positioning the IC on a circuit board that is populated with peripheral devices, which would be present during actual operation of the IC, into the method of Soh, as taught by Mok, with the motivation, as stated by Mok (column #22, lines #13 through 18), to allow the test and burn of

integrated circuit dice (items #44 & 100) after packaging and singulation (Item #122), making it possible to detect assembly, saw and handling caused defects, while keeping the die in position for precision handling with massive parallelism.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 4, 6, 7, 12-26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Mok et al. (U.S. Pat. No.6,791,171 , Patented 09/14/04, Filed 06/28/02) and Soh et al. (U.S. Pat. No.6,060,895 , Patented 05/09/00, Filed 04/20/98), as applied to claims 1, 8-11 above, in view of Gold et al. (U.S. Pub. No.2003/0158697, Pub Date 08/21/03, Filed 02/19/02).

Mok and Soh substantially show, in the corresponding test, a method for preparing an integrated circuit for thermal testing, as shown in the claims listed above.

Mok shows, ***pertaining to claim #6,*** a method further comprising the step of providing a temperature controller coupled to the temperature generation device and the temperature sensor **(column 23, lines 19-28)**. ***Pertaining to claim #14,*** Mok shows a method further comprising the steps of: initializing a test of the IC, including presetting a target temperature to be maintained at the IC **(column 23, lines 19-28)**; enabling and regulating the temperature generation device until the temperature at the IC reaches the target temperature; initializing a functional test for the IC;

and offsetting changes in the temperature at the IC with a change in regulation of the temperature generation device to achieve the target temperature during the functional test to the IC **(column 23, lines 19-28).** ***Pertaining to claim #18,*** Mok shows a method for thermally assisted testing of an integrated circuit (1C), the method comprising **(column 9, lines 66-67; column 10, lines 1-34)**: (a) setting a target temperature to be generated by a temperature generation device located within the IC **(column 33, lines 12-19)**; (b) operating the temperature generation device to generate the target temperature **(column 23, lines 19-28).** ***Pertaining to claim #20,*** Mok shows a method according to claim 19, comprising the more specific step of using the temperature controller to adjust the target temperature depending on the temperature associated with the IC, and to instruct the temperature generation device to generate the target temperature **(column 23, lines 19-28).** ***Pertaining to claim #21,*** Mok shows a method according to claim 18, further comprising the step of initializing a functional test of the IC **(column 15, lines 29-44).** ***Pertaining to claim #24,*** Soh shows a system for thermally assisted testing of an integrated circuit (IC), comprising: a temperature generation device located within the IC and configured for a primary purpose of affecting a temperature at the IC; and a temperature controller coupled to the temperature generation device **(fig. 2, 2a and 5; column 3, lines 63-67; column 4, lines 1-11 and line 33-44; column 5, lines 57-67; column 6, lines 1-12).**

Mok and Soh fail to show, with respect to **claim #6**, a temperature sensor. Mok fails to show, with respect to **claim #14**, enabling the temperature sensor. Mok fails to show, with respect to **claim #18**, (c) operating the IC; (d) sensing a temperature associated with the IC; and (e) adjusting the target temperature of the temperature generation device relative to the

temperature associated with the IC. Mok fails to show, with respect to **claim #24**, a temperature sensor located within close proximity to the IC' and to the temperature sensor.

Gold teaches, in a similar method, a technique for preparing an integrated circuit for thermal testing.

Gold teaches, ***pertaining to claim #3***, a method, further comprising the step of positioning a temperature sensor within close proximity to the IC **(pg; #1, paragraph 0005)**. ***Pertaining to Claim #4***, Gold also teaches, a method, comprising the more specific step of positioning the temperature sensor within the IC **(pg; #1, paragraph 0005)**. ***Pertaining to claim #6*** Gold shows a method comprising a temperature sensor **(pg; #1, paragraph 0007)**. ***Pertaining to claim #7***, Gold shows a method comprising the more specific step of positioning the temperature controller within the IC **(pg; #2, paragraph 0024)**. ***Pertaining to claim #12***, Gold shows a method, including the more specific step of sensing the temperature at the IC using a temperature sensor located within close proximity to the IC **(pg; #1, paragraph 0005)**. ***Pertaining to claim #13***, Gold shows method including the more specific step of sensing the temperature at the IC using a temperature sensor located within the IC **(pg; #1, paragraph 0005)**. ***Pertaining to claim #14***, Gold shows enabling the temperature sensor **(pg; #1, paragraph 0007)**. ***Pertaining to claim #15***, Gold shows a method further comprising the step of applying the temperature sensor to communicate in real-time with an integrally formed power management unit used with the IC for a primary purpose of adjusting voltage levels **(pg; #1, paragraph 0005; pg; #4, paragraph 0036)** and frequency of the IC **(pg. 3&4, paragraph 0031, paragraph 0036)**. ***Pertaining to claim #16***, Gold shows a method further comprising the step of

communicating the temperature at the IC to a temperature controller **(pg; #1, paragraph 0005)**. ***Pertaining to claim #17,*** Gold shows a method further comprising the step of predefining a maximum allowable temperature for the IC **(pg; #1, paragraph 0007)**. ***Pertaining to claim #18,*** Gold shows a method, (c) operating the IC **(pg; #2, paragraph 0021)**; (d) sensing a temperature associated with the IC **(pg; #1, paragraph 0005 and 0007)**; and (e) adjusting the target temperature of the temperature generation device relative to the temperature associated with the IC **(pg; #1, paragraph 0005, 0007)**. ***Pertaining to claim #19,*** Gold shows a method, further comprising the step of communicating the temperature associated with the IC to a temperature controller **(pg; #1, paragraph 0005)**. ***Pertaining to claim #22,*** Gold shows a method, further comprising the step of configuring the temperature controller to maintain the temperature associated with the IC at a substantially constant temperature by offsetting changes in the temperature associated with the IC and any peripheral devices with a change in the target temperature to be generated by the temperature generation device **(pg; #1&3, paragraph 0024, paragraph 0025)**. ***Pertaining to claim #23,*** Gold shows a method, comprising the more specific step of sensing a temperature associated with the IC, using a temperature sensor located within the IC **(pg; #1, paragraph 0005)**. ***Pertaining to claim #24,*** Gold shows a temperature sensor located within close proximity to the IC' and to the temperature sensor **(pg; #1, paragraph 0005)**. ***Pertaining to claim #25,*** Gold shows a system, wherein the device is also comprised of a power management unit electronically coupled to the temperature sensor and configured for adjusting voltage levels and frequency of the IC **(pg; #1, paragraph 0005; pg; #4, paragraph 0036)**, wherein the power management unit communicates in real-time with the temperature sensor **(pg; #3&4, paragraph 0031, paragraph 0036)**. ***Pertaining to claim #26,*** Gold shows a

system, wherein the temperature sensor is installed within the IC **(pg; #2, paragraph 0024)**. ***Pertaining to claim #28,*** Gold shows a system, wherein the temperature controller is installed within the IC **(pg; #2, paragraph 0024)**.

It would have been obvious to one having ordinary skill in the art at the time the invention was made, with respect to **claim #3, 4, 6, 7, 12, 13, 14, 23, 24, 26, and 28**, to include a temperature sensor either within or in close proximity to the IC, into the method of Mok, as taught by Gold, with the motivation that placing the sensor close or within the IC would produce the most reliable results to be used for control.

It would have been obvious to one having ordinary skill in the art at the time the invention was made, with respect to **claim #16 and 19**, to include the step of communicating the temperature at the IC to a temperature controller, into the method of Mok, as taught by Gold, with the motivation that the communication of the existing temperature to a controller would allow the fastest feed back information for controlling the temperature.

It would have been obvious to one having ordinary skill in the art at the time the invention was made, with respect to **claim #15 and 25**, to include wherein the device is also comprised of a power management unit electronically coupled to the temperature sensor and configured for adjusting voltage levels and frequency of the IC, into the method of Mok, as taught by Gold, with the motivation that by allowing the device to control the voltage levels and frequency of the IC, a better control of the over all temperature of the IC can be obtaining.

It would have been obvious to one having ordinary skill in the art at the time the invention was made, with respect to **claim #18**, to include (c) operating the IC (d) sensing a temperature associated with the IC; and (e) adjusting the target temperature of the temperature generation device relative to the temperature associated with the IC, into the method of Mok, as taught by Gold, with the motivation that this allows the controller to observe the IC and control the environment of the operation.

It would have been obvious to one having ordinary skill in the art at the time the invention was made, with respect to **claim #22**, to include the step of configuring the temperature controller to maintain the temperature associated with the IC at a substantially constant temperature by offsetting changes in the temperature associated with the IC and any peripheral devices with a change in the target temperature to be generated by the temperature generation device, into the method of Mok, as taught by Gold, with the motivation that by allowing the controller and the temperature generation device to work together produces an advantage to controlling the over all environment of the IC.

Allowable Subject Matter

Claim #2, 5, 27, 29 and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim #2 allowable subject matter, pending further search.

✓ Providing user with instructions to operate the temperature generation device

Claim #5 allowable subject matter, pending further search.

✓ Multiple temperature generation devices.

Claim #27 allowable subject matter, pending further search.

✓ Multiple temperature generation devices.

Claim #29 allowable subject matter, pending further search.

✓ Initializing a functional test for the IC.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre' Stevenson whose telephone number is (571) 272 1683. The examiner can normally be reached on Monday through Friday from 7:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt, can be reached on (571) 272 1873. The fax phone number for the organization where this application or proceeding is assigned is (703) 308 7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 0956. Also, the proceeding numbers can be used to fax information through the Right Fax system;

(703) 872-9306

Andre' Stevenson

Art Unit 2812

10/31/05

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER